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US 6055160 A	20000425	High temperature oven electrical feed through	361/742	Schmidt, Glen Eugene et
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US 5870274 A	19990209	Capacitive PCB with internal capacitive laminate	361/311	Lucas, Gregory L.
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L Number	Hits	Search Text	DB	Time stamp
1	8856	printed adj circuit adj board and multi$1layer	USPAT; EPO; JPO	2004/02/18 12:06
2	386	(printed adj circuit adj board and multi$1layer) and signal adj (plane layer) and (ground power reference) adj (plane layer)	USPAT; EPO; JPO	2004/02/18 12:07
3	22	("3739469" | "4170819" | "4211603" | "4675788" | "4679872" | "5057809" | "5225969" | "5374788" | "5376759" | "5421083" | "5459642" | "5565262" | "5612660" | "5808529" | "5823795" | "5847451" | "5853303" | "5876842" | "5921815" | "5949030" | "6019639" | "6228511").PN.	USPAT	2004/02/18 12:09
4	7	("5006820" | "5281151" | "5451721" | "5686764" | "6194668" | "6271478" | "6335493").PN.	USPAT	2004/02/18 12:13
5	7	("5363280" | "5371653" | "5451720" | "5473813" | "5590030" | "5743004" | "6080012").PN.	USPAT	2004/02/18 12:14
6	6	5743004.URPN.	USPAT	2004/02/18 12:15
7	3	("5281151" | "5451721" | "5686764").PN.	USPAT	2004/02/18 12:18
8	29	4511950.URPN.	USPAT	2004/02/18 12:31
9	13	("4328530" | "4450029" | "4511950" | "4575745" | "4616292" | "4628411" | "4647877" | "4694123" | "5102352" | "5136471" | "5418690" | "5451720" | "5523921").PN.	USPAT	2004/02/18 12:32
12	10	5930119.URPN.	USPAT	2004/02/18 14:09
13	9	("4362899" | "4738632" | "4879433" | "5365406" | "5509066" | "5541369" | "5568361" | "5696667" | "5764489").PN.	USPAT	2004/02/18 14:10
16	24	4675789.URPN.	USPAT	2004/02/18 14:14
17	6	("3519959" | "3568000" | "3680005" | "3740678" | "4362899" | "4498122").PN.	USPAT	2004/02/18 14:18
20	27	3740678.URPN.	USPAT	2004/02/18 14:27
21	932	174/$.ccls. and dielectric and (signal ground power) adj (plane layer core)	USPAT; EPO; JPO	2004/02/18 16:49
22	211	(174/$.ccls. and dielectric and (signal ground power) adj (plane layer core)) and laminat$4 and copper with thick$4	USPAT; EPO; JPO	2004/02/18 16:39
23	49	257/7$.ccls. and dielectric and (signal ground power) adj (plane layer core) and lamination and (copper cu) with thickness	USPAT; EPO; JPO	2004/02/18 16:51
24	79	361/7$.ccls. and dielectric and (signal ground power) adj (plane layer core) and lamination and (copper cu) with thickness	USPAT; EPO; JPO	2004/02/18 16:53
25	43	438/$.ccls. and dielectric and (signal ground power) adj (plane layer core) and lamination and (copper cu) with thickness	USPAT; EPO; JPO	2004/02/18 16:54
26	13	333/$.ccls. and dielectric and (signal ground power) adj (plane layer core) and lamination and (copper cu) with thickness	USPAT; EPO; JPO	2004/02/18 16:55
-	6	backplane.ti. and goergen.in.	USPAT; US-PGPUB; EPO; JPO	2004/02/09 18:56
-	673	multi$1layer adj circuit with board and laminat$3 and through adj hole	USPAT; EPO; JPO	2004/02/09 18:57
-	83	(multi$1layer adj circuit with board and laminat$3 and through adj hole) and (copper power signal) adj layer same dielectric	USPAT; EPO; JPO	2004/02/09 18:58

-	1	5311406.pn.	USPAT; EPO; JPO	2004/02/09 19:00
-	64	29/$.ccls. and multi$1layer with (substrate board) and (dielectric insulat$3) adj layer and laminat$4 and power adj (plane layer)	USPAT; EPO; JPO	2004/02/13 15:45
-	13	(backplane back$1plane) and multi$1layer with (substrate board) and (dielectric insulat$3) adj layer and laminat$4 and power adj (plane layer)	USPAT; EPO; JPO	2004/02/13 15:48
-	124	stack$3 and multi$1layer with (substrate board) and (dielectric insulat$3) adj layer and laminat$4 and power adj (plane layer)	USPAT; EPO; JPO	2004/02/13 15:58
-	299	circuit adj board and stack$3 and multi$1layer with (substrate board) and (dielectric insulat$3) adj (film layer plane material) and laminat$4 and (ground power) adj (plane layer film)	USPAT; EPO; JPO	2004/02/13 16:17
-	268	circuit adj board and stack$3 and multi$1layer with (substrate board) and (dielectric insulat$3) adj (film layer plane material) and laminat$4 and (ground power signal) adj (plane layer film) and copper	USPAT; EPO; JPO	2004/02/13 16:19
-	26	three with (ounce oz) with copper with (layer film plane)	USPAT; EPO; JPO	2004/02/13 16:51
-	1	4891616.pn.	USPAT; EPO; JPO	2004/02/17 11:47
-	1	6081340.pn.	USPAT; EPO; JPO	2004/02/17 11:48
-	1	5010641.pn.	USPAT; EPO; JPO	2004/02/17 11:48
-	1	5870274.pn.	USPAT; EPO; JPO	2004/02/17 11:49
-	1	5566083.pn.	USPAT; EPO; JPO	2004/02/17 11:49
-	1	5261153.pn.	USPAT; EPO; JPO	2004/02/17 11:50
-	1	4694123.pn.	USPAT; EPO; JPO	2004/02/17 11:50
-	1	6030693.pn.	USPAT; EPO; JPO	2004/02/17 11:50
-	1	5311406.pn.	USPAT; EPO; JPO	2004/02/17 11:51
-	1	6229095.pn.	USPAT; EPO; JPO	2004/02/17 11:51
-	1	5397861.pn.	USPAT; EPO; JPO	2004/02/17 11:52
-	1	6015300.pn.	USPAT; EPO; JPO	2004/02/17 11:52
-	1	5841074.pn.	USPAT; EPO; JPO	2004/02/17 11:53
-	1	4862161.pn.	USPAT; EPO; JPO	2004/02/17 11:53
-	1	5548734.pn.	USPAT; EPO; JPO	2004/02/17 11:53
-	1	5308926.pn.	USPAT; EPO; JPO	2004/02/17 11:54
-	1	5682298.pn.	USPAT; EPO; JPO	2004/02/17 11:54
-	1	6091609.pn.	USPAT; EPO; JPO	2004/02/17 11:55
-	1	6181004.pn.	USPAT; EPO; JPO	2004/02/17 11:55
-	1	6333981.pn.	USPAT; EPO; JPO	2004/02/17 12:06
-	1	6573600.pn.	USPAT; EPO; JPO	2004/02/17 12:06
-	2	5841074.URPN.	USPAT	2004/02/17 14:32

-	13	("4328530" | "4450029" | "4511950" | "4575745" | "4616292" | "4628411" | "4647877" | "4694123" | "5102352" | "5136471" | "5418690" | "5451720" | "5523921").PN.	USPAT	2004/02/17 14:32
-	6	6181004.URPN.	USPAT	2004/02/17 14:34
-	70	("4100377" | "4645872" | "4771425" | "4802199" | "4843606" | "4866704" | "4886704" | "4896350" | "4964159" | "4969184" | "5068888" | "5159592" | "5185502" | "5208806" | "5208811" | "5212691" | "5309437" | "5327486" | "5333188" | "5341374" | "5343517" | "5375118" | "5400068" | "5406557" | "5406620" | "5428608" | "5430727" | "5432848" | "5432907" | "5438565" | "5440554" | "5444477" | "5457684" | "5463625" | "5469504" | "5473680" | "5479487" | "5481600" | "5491693" | "5511114" | "5519704" | "5521914" | "5526353" | "5533018" | "5541917" | "5541927" | "5553063" | "5561670" | "5563937" | "5572643" | "5583920" | "5590181" | "5604737" | "5608446" | "5608786" | "5610910" | "5636216" | "5646982" | "5712907" | "5724355" | "5742596" | "5742670" | "5790548" | "5867495" | "5889774" | "5894512" | "6103135" | "6131279" | "6181004" | "6255039").PN.	USPAT	2004/02/17 14:40
-	1180	multi$1layer with circuit adj board and (ground signal power) adj (plane layer film)	USPAT; EPO; JPO	2004/02/17 18:05
-	463	(multi$1layer with circuit adj board and (ground signal power) adj (plane layer film)) and dielectric and laminat$3	USPAT; EPO; JPO	2004/02/17 18:06
-	395	((multi$1layer with circuit adj board and (ground signal power) adj (plane layer film)) and dielectric and laminat$3) and copper	USPAT; EPO; JPO	2004/02/17 18:06
-	20	(((multi$1layer with circuit adj board and (ground signal power) adj (plane layer film)) and dielectric and laminat$3) and copper) and (polyphenylene FR-4 adj1 resin)	USPAT; EPO; JPO	2004/02/17 18:07
-	233	(((multi$1layer with circuit adj board and (ground signal power) adj (plane layer film)) and dielectric and laminat$3) and copper) and (polyphenylene resin)	USPAT; EPO; JPO	2004/02/17 18:09

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1 **Radiation from printed circuit board edge structures**
Gisin, F.; Pantic-Tanner, Z.;
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2 **Wiring statistics and printed wiring board thermal conductivity**
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3 **Ground starvation effects on multi-layer PCBs**
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4 **Investigation of the effectiveness of DC power bus interplane capacitance in reducing radiated EMI from multi-layer PCBs**
O'Sullivan, C.B.; Musladin, M.;
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5 **Multichip Packaging Design for VLSI-Based Systems**
Bartlett, C.; Segelken, J.; Teneketges, N.;
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6 **Simplified modeling of parallel plate resonances on multilayer printed circuit boards**
Tarvainen, T.;
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7 **Reduction in radiated emission by symmetrical power-ground layer stack-up PCB with no open edge**
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8 **Improving signal integrity in circuit boards by incorporating absorbing materials**
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9 **Simultaneous switching noise suppression for high speed systems using embedded decoupling**
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10 **Composite effects of reflections and ground bounce for signal vias in multi-layer environment**
Sheng-Mou Lin; Ruey-Beei Wu;
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11 **EMI resulting from signal via transitions through the DC power bus**
Wei Cui; Xiaoning Ye; Archambeault, B.; White, D.; Min Li; Drewniak, J.L.;
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12 **Escape routing from chip scale packages**
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13 **Thermal evaluation of Θ_{JA} for varying board conductivity**
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14 **High-leadcount, single- and multi-metal-layer TAB: design considerations**
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15 **Enhanced high speed performance from HDI thin film multichip modules**
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2 **A compact multilayer IC package model for efficient simulation, analysis, and design of high-performance VLSI circuits**
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7 **Characterization of peripheral and core SSOs in a flip-chip package**
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11 **Multichip Packaging Design for VLSI-Based Systems**
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